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(19) (CA) **CANADIAN PATENT** (12)

(54) Integrated Communications System for HDLC
Variable-Length Data Packets and Fixed-Length
Voice/Video Packets

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ABSTRACT OF THE DISCLOSURE

1 In an Integrated communications system, HDLC variable-length
2 packets and non-HDLC fixed-length packets are decomposed into cells
3 and a cell Identifier is generated for each of the cells for identifying its
4 type. A frame sync code is transmitted from one end of a transmission
5 channel, and the cell identifier and each of the cells are assembled into
6 a field and a plurality of such fields are assembled into a frame for
7 transmission. The frame sync code is detected at the other end of the
8 transmission channel as a timing reference and the frame is
9 deassembled into fields in response to the timing reference and each
10 field is deassembled into a cell Identifier and a cell. According to each
11 deassembled cell Identifier, the cells of each field are composed into the
12 original HDLC variable-length packet or non-HDLC fixed-length packet.

1 TITLE OF THE INVENTION

- 2 "Integrated Communications System For HDLC Variable-Length Data
3 Packets And Fixed-Length Voice/Video Packets"

4 TECHNICAL FIELD

5 The present invention relates generally to communications system
6 which integrates signals of different formats, and more particularly to a
7 communications system which integrates HDLC (high level data link
8 control) variable-length data packets with non-HDLC fixed-length
9 packets. The HDLC packet is transmitted according to the CCITT
10 (International Telegraph and Telephone Consultative Committee)
11 Recommendation X. 25 protocol which involves packet retransmission
12 for error correction, while the non-HDLC fixed-length packets such as
13 voice and/or video packets are transmitted involving no packet
14 retransmission in the event of an error.

15 BACKGROUND OF THE INVENTION

16 In a prior art Integrated communication system in which HDLC X. 25
17 computer data packets and fixed-length voice/video packets are
18 transmitted over a common transmission medium, the fixed-length
19 packets are transformed into the HDLC format and a specified Identifier
20 is inserted into the address or control field of the transformed packets so
21 that both types of packets are treated at the receive end as variable-
22 length packets. Because of the adoption of the HDLC format for mixing
23 the different formats, the prior art system employs what is called "zero-
24 insertion and zero-deletion" scheme by forcibly inserting a 0 bit if there
25 is a string of five consecutive 1 bits at the transmit end and removing it at
26 the receive end to allow transmission of a flag pattern "01111110" as a
27 delimiter of the variable-length packet.

28 However, if disruption occurs in a received data stream causing an



1 error in the inserted 0 bit, the packet containing this error bit is aborted.
2 Otherwise, such a packet propagates along the network as a truncated,
3 short packet or merges with a preceding packet resulting in a long
4 packet. In either case, the packet is detected as an error by a frame
5 check sequence and is eventually discarded. If an error occurs in X. 25
6 HDLC packet, it can be corrected by the packet retransmission scheme,
7 whereas voice/video packets in error are simply discarded. The
8 potential source of this type of error is the bit reversal of the forcibly
9 inserted 0 bit in the voice/video packet. Such irrecoverable errors can
10 occur at 2.1-second intervals for a transmission rate of 1.5 Mbps at a bit
11 error rate of 10^{-5} . One approach to this problem is to append an error
12 correcting code to fixed-length packets. However, since the beginning
13 and ending points of such packets cannot be guaranteed with a high
14 degree of certainty, the error correcting code approach serves no
15 purpose. Another approach would be to employ a retransmission
16 scheme as in the case of the X.25 packets. However, the real-time
17 transmission requirement of the voice/video packet cannot be met by
18 the retransmission scheme.

19 SUMMARY OF THE INVENTION

20 It is therefore an object of the present invention to provide an
21 integrated communications system for HDLC variable-length data
22 packets and non-HDLC fixed-length voice/video packets which is
23 capable of significantly reducing the error rate of the non-HDLC packets.

24 According to the present invention, HDLC variable-length packets
25 and non-HDLC fixed-length packets are decomposed into one or more
26 cells and a cell identifier is generated for each of the cells for identifying
27 type of the packet from which said cell is decomposed. A frame sync
28 code is transmitted from one end of a common transmission medium,

1 and the cell identifier and each of the cells are assembled into a field
2 and a plurality of such fields are assembled into a frame, which is
3 transmitted through the transmission medium. The frame sync code is
4 detected at the other end of the transmission medium as a timing
5 reference and the frame is deassembled into fields in response to the
6 timing reference. Each of the fields is deassembled into a cell identifier
7 and a cell. According to each deassembled cell identifier, the cells of
8 each field are composed into the original HDLC variable-length packet
9 or non-HDLC fixed-length packet.

10 More specifically, the present invention provides an integrated
11 communications system. The transmit end of the system comprises an
12 HDLC variable-length packet transmitter and a non-HDLC fixed-length
13 packet transmitter. A shift register is provided having an input terminal
14 connected to the packet transmitters and an output terminal connected
15 to one end of a transmission medium. A sync generator supplies a sync
16 code to the shift register at periodic intervals. A cell formatter activates
17 for a predetermined period one of the packet transmitters having a
18 packet to transmit so that a portion of the packet is supplied to the shift
19 register as a cell. The cell formatter causes a head generator to supply
20 a cell identifier identifying type of the packet from which said cell is
21 decomposed to the transmit shift register to form a field with the cell,
22 and causes the shift register to assemble the sync code and a plurality
23 of fields into a frame for transmission. At the receive end of the system,
24 a shift register is provided having an input terminal connected to the
25 transmission medium. A sync detector detects the sync code contained
26 in the frame supplied to the shift register. A header detector is
27 responsive to a sync code detected by the sync detector for detecting
28 the cell identifier of each field of the frame. An HDLC variable-length

1 packet receiver and a non-HDLC fixed-length packet receiver are
2 provided. A cell deformatter is responsive to the cell identifier detected
3 by the header detector for activating one of the packet receivers
4 identified by the detected cell identifier so that each cell is supplied from
5 the shift register to the identified packet receiver where the cells are
6 composed into the original packet.

7 BRIEF DESCRIPTION OF THE DRAWINGS

8 The present invention will be described in further detail with
9 reference to the accompanying drawings, in which:

10 Fig. 1 is a block diagram of a transmit section of the integrated
11 communications system of the present invention;

12 Figs. 2A and 2B are a flowchart illustrating details of the cell
13 formatter of Fig. 1;

14 Figs. 3A, 3B and 3C are timing diagrams for generating frames
15 respectively for HDLC, 360-bit and 1080-bit packets; and

16 Fig. 4 is a block diagram of a receive section of the system.

17 DETAILED DESCRIPTION

18 Referring now to Fig. 1, there is shown a transmit section of the
19 integrated communications system of the present invention. According
20 to this invention, variable-length packets such as X.25-protocol HDLC
21 data packets and fixed-length voice or video packets such as 360-bit
22 length or 1080-bit length are decomposed into segments of 360-bit
23 length each, which are called in this specification as "cells." Four such
24 cells are interleaved with 8-bit cell identifier, or cell identifiers (CID) to
25 form "fields" which are encapsulated between 8-bit sync fields, instead
26 of the usual "01111110" flag patterns, to form a 1480-bit length frame.
27 The HDLC packets and the variable length packets are shown as being
28 generated by a processor 10 and supplied to respective packet

1 transmitters 11, 12 and 13 for transmission to a destination processor,
2 not shown. Packet transmitters 11, 12 and 13 are provided with
3 respective memories for storing the generated packets, each of these
4 memories being driven by a sequence of 360 clock pulses which is
5 extracted by a clock distributor 14 from a continuous stream of clock
6 pulses supplied from a clock source 15.

7 If there is a packet to transmit, packet transmitters 11, 12 and 13
8 place a request for transmission through respective lines 11A, 12A, 13A
9 to a priority circuit 16 which selects one of the requests according to a
10 predetermined decision algorithm. If a plurality of requests exist
11 simultaneously. The type of a packet selected by priority circuit 16 is
12 notified to a cell formatter 17. The clock pulse from source 15 is
13 supplied to a 1480-bit counter 18 to cause it to supply timing
14 information to cell formatter 17 and to a sync generator 19 which
15 generates an 8-bit frame sync at intervals of 1480 bits and writes it into a
16 shift register 22 which is shifted at the clock rate.

17 An 8-bit cell identifier generator 20 is provided for writing an 8-bit
18 cell identifier (CID) into shift register 22 at 368-bit intervals in response to
19 a control signal supplied from cell formatter 17. The 8-bit cell identifier
20 of each cell indicates the type of the packet from which the cell is
21 derived. The cell identifier is a block code encoded with error
22 correcting bits. To allow detection and correction of errors, the
23 Hamming distance of 3 bits or more is secured between cell identifiers.
24 Four cell identifiers are provided: CID="0" (which is encoded as
25 "10101001") identifying cells derived from the HDLC packet, CID="1"
26 ("11010100") identifying cells derived from the 360-bit fixed-length
27 packet, CID="2" ("01011011") identifying each of the first and second
28 cells of the 1060-bit fixed length packet, and CID="3" ("00100110")

1 identifying the third cell of the 1060-bit packet.

2 Cell formatter 17 further controls clock distributor 14 and a
3 multiplexer 21 through bus 23. Multiplexer 21 terminates the data
4 outputs of packet transmitters 11, 12 and 13 for selectively coupling cell
5 data bits to the shift register 22. A flag generator 24 is also connected
6 to respond to a signal from cell formatter 17 to write a flag sequence
7 "0111110" into shift register 22 when no data packet is present. The
8 details of cell formatter 17 are shown in the flowchart of Figs. 2A and 2B.

9 Program execution begins with initializing steps 30 and 31 to reset
10 variables N and F to zero, where variable N represents the serial number
11 of each cell in a given frame and $F=1$ indicates that there is no call
12 request in any of packet transmitters. Control then enters a search loop
13 comprising steps 32, 33, 34 and 35 for detecting whether there is a call
14 request, and if so which one of the packet transmitters is requesting the
15 call. If a call is requested by HDLC packet transmitter 11, control passes
16 through steps 32, 33, 34 and enters step 40 to check to see if a variable
17 N is equal to zero or not. If the answer is affirmative, exit is to step 41 to
18 wait until a sync code is transmitted, and if the answer is negative, exit is
19 to step 42 to supply a cell identifier code $CID="0"$ to the 8-bit CID
20 generator 20 to cause it to write an 8-bit cell identifier "10101001" into
21 shift register 22 at the clock count of $(8 + 368 \times N)$ bits. Thus, cell
22 identifiers of each frame are successively transmitted at clock counts of
23 8, 376, 744, and 1112 bits, respectively, following the transmission of a
24 frame sync 80 generated by sync generator 19 (Fig. 3A). Following the
25 transmission of a cell identifier, control proceeds to decision step 43 to
26 determine if $F = 1$ exists. If there is none, control proceeds to step 44 to
27 supply the $CID="0"$ code to bus 23 for a period of 360 clock bits. In
28 response to $CID="0"$, clock distributor 14 establishes a path leading to

1 the HDLC packet transmitter 11 for a 360-bit duration to supply 360
2 clock pulses to HDLC packet transmitter 11. Concurrently, multiplexer 21
3 responds to CID="0" by establishing a path from HDLC packet
4 transmitter 11 to shift register 22 during the same duration. HDLC
5 packet transmitter 11 is driven by the clock pulses from distributor 14 to
6 supply cell data #1 from its memory to shift register 22.

7 Exit then is to step 45 in which the variable N is incremented by one.
8 Variable N is checked in step 46 to see if $N = 4$, or not. If not, control
9 returns to the search loop to repeat the process so that, as long as a call
10 request from HDLC packet transmitter 11 is present, succeeding cell data
11 #2, #3 and #4 of the HDLC packet are sequentially delivered from HDLC
12 packet transmitter 11 to shift register 22, respectively following cell
13 identifiers CID="0." The transmission of a 1480-bit frame of HDLC data
14 completes when N becomes equal to 4. When decision in step 46 goes
15 affirmative, exit is to step 47 which resets N to zero so that control is
16 caused to delay the transmission of the CID of first occurrence in each
17 frame by step 41 until a frame sync is transmitted.

18 If a call is requested from 360-bit packet transmitter 12, control exits
19 the search loop and enters a subroutine comprising steps 50 to 52
20 which are respectively similar to steps 40 to 42 just described, with the
21 exception that in step 52 cell identifier CID="1" is supplied to CID
22 generator 20. Control advances to step 53 to supply the code CID="1"
23 to bus 23 for a 360-bit duration. Therefore, an 8-bit cell identifier
24 "11010100" is written into shift register 22, following a frame sync code
25 90 (Fig. 3B). In response to CID="1", clock distributor 14 establishes a
26 path leading to the 360-bit packet transmitter 12 to drive it for a 360-bit
27 duration. Concurrently, multiplexer 21 responds to CID="1" by
28 establishing a path from 360-bit packet transmitter 12 to shift register 22.

1 Step 53 is followed by steps 45 to 47 as in the case of HDLC packets to
2 repeat the transmission of succeeding cell data. If several 360-bit
3 packets exist as shown in Fig. 3B, steps 50 to 53 are repeatedly executed
4 until $N = 4$ is obtained in step 46.

5 If 1080-bit packet transmitter 13 has two 1080-bit packets 101 and
6 102 to transmit, for example (see Fig. 3C), control enters step 60 to reset
7 a variable i to zero. Step 60 is followed by steps 61 to 64 which are
8 similar to steps 50 to 53, respectively, with the exception that in step 63
9 cell identifier code $CID="2"$ is supplied to CID generator 20 and in step
10 64 the code $CID="2"$ is supplied to bus 23 for a 360-bit duration.
11 Therefore, an 8-bit cell identifier "01011011" is written into shift register
12 22, following a frame sync code 100 (Fig. 3C). In response to cell
13 identifier code $CID="2"$, clock distributor 14 establishes a path leading to
14 the 1080-bit packet transmitter 13 to drive it for a 360-bit duration.
15 Concurrently, multiplexer 21 responds to code $CID="2"$ by establishing
16 a path from 1080-bit packet transmitter 13 to shift register 22. In this
17 way, a cell identifier $CID="2"$ and cell data #1-1 of 1060-bit packet 101
18 are successively transmitted.

19 Step 64 is followed by step 65 which increments the variable N by
20 one. Variable N is checked in step 66 to see if $N = 4$, or not. If N is not
21 equal to 4, control advances to step 67 to increment the variable i by
22 one, and if $N = 4$, exit is to step 68 to reset the variable N to zero before
23 executing step 67. Following step 67, step 69 is executed by
24 determining if $i = 2$. If not, control returns to step 61 to repeat the
25 process so that cell data #1-2 of 1080-bit packet 101 is transmitted
26 following a cell identifier $CID="2"$. After transmission of two cell data
27 preceded by cell identifiers $CID="2"$, variable i has been incremented to
28 2, and control exits from step 69 and enters steps 70 to 73 which are

1 similar to steps 61 to 64 with the exception that in step 72 cell identifier
2 code CID="3" is supplied to CID generator 20 and in step 64 code
3 CID="3" is supplied to bus 23 for 360-bit duration. Therefore, an 8-bit
4 cell identifier "00100110" is written into shift register 22, following cell
5 data #1-2. In response to CID="3", clock distributor 14 maintains the
6 previous path leading to the 1080-bit packet transmitter 13 to drive it for
7 a 360-bit duration. Concurrently, multiplexer 21 responds to CID="3"
8 by maintaining the previous path from 1080-bit packet transmitter 13 to
9 shift register 22. In this way, a cell identifier CID="3" and cell data #1-3
10 of 1060-bit packet 101 are successively transmitted.

11 Exit from step 73 is to steps 44 to 46. Variable N is incremented and
12 checked for N = 4. After transmission of the 1080-bit packet 101, N = 3
13 is obtained and control exits from step 45 and reenters the search loop
14 to detect whether a call request is still present. Since the 1080-bit packet
15 102 is waiting in transmitter 13 to be processed, steps 60 to 69 are
16 looped twice for transmitting cell data #2-1 and #2-2 of packet 102 and
17 steps 70 to 74 are executed once for transmitting cell data #2-3 of the
18 packet. Because N = 3 at the instant cell data #2-1 is transmitted, step 62
19 skipped in the first pass, but because of the subsequent increment in
20 step 65 to N=4, step 62 is executed in the second pass to allow for
21 insertion of a frame sync 103 before transmitting a cell identifier 104
22 which precedes cell data #2-2. Execution of steps 70 to 73 follows to
23 sequentially transmit a cell identifier 105 and cell data #2-3 of packet
24 102.

25 If there is no call request, control leaves the search loop and enters
26 step 36 to set variable F to 1 and proceeds through steps 40 to 42 to
27 transmit a or cell identifier CID="0" and exits from step 43 to step 48 to
28 cause flag generator 24 to write a cyclic pattern of flag sequences

1 "01111110" into shift register 22. Exit then is to step 49 to reset variable
2 F to 0, which is followed by step 45. Therefore, if there is no packet to
3 transmit following the transmission of the second 1080-bit packet 102,
4 flag sequences are transmitted respectively preceded by cell identifiers
5 identical to those preceding the cell data of HDLC packets.

6 It will be seen from the above that the segmented 360-bit cell data
7 of different types of packet can be transmitted continuously by allowing
8 them to be encapsulated between frame sync codes.

9 Fig. 4 is a block diagram of a receive section of the integrated
10 communications system of the present invention. The cell-formatted
11 data stream is clocked into a shift register 200 by a clock recovery circuit
12 201, which also drives a clock counter 202. Shift register 200 supplies its
13 contents in parallel form to a sync detector 203 and a cell identifier
14 detector 204. On detecting each sync, sync detector 203 resets the
15 clock counter 202. The CID detector 204 comprises a 256-bit read-only
16 memory having an 8-bit address input. The ROM 205 stores 256
17 possible binary states. Since the cell identifier is an 8-bit block code with
18 a Hamming distance of 3 bits or more, two-bit errors in the received
19 block code can be corrected in the ROM 205 by translating the
20 corrupted 8-bit cell identifier to an original 8-bit code.

21 A cell deformatter 205 provides deformatting control over the
22 received data according to a clock count supplied from counter 202. In
23 response to predetermined clock counts, cell deformatter 205 enables
24 the CID detector 204 to read out a two-bit cell identifier code into cell
25 deformatter 205. In response to a read cell identifier, cell deformatter
26 205 supplies a code to a clock distributor 206 in a manner similar to the
27 transmit section of the system so that clock pulses of 360-bit duration
28 from clock recovery circuit 201 are supplied to one of HDLC packet

1 receiver 207, and 360-bit and 1080-bit packet receivers 208 and 209 to
2 selectively receive cell data from the output of shift register 200. Each of
3 the packet receivers assembles the cell data into the original packet
4 format for coupling to the data processor 10.

5 Since the fixed-length packets are not converted into HDLC format,
6 data preceded by cell identifiers CID="1", "2" and "3" are not aborted
7 even if they are corrupted. Instances in which data is aborted due to
8 reversal of an inserted zero bit occur only with respect to HDLC data,
9 i.e., data sent with cell identifier CID="0." The rate of fixed-length data
10 being discarded as an error can therefore be significantly reduced in
11 comparison with the prior art system.

12 The foregoing description shows only one preferred embodiment
13 of the present invention. Various modifications are apparent to those
14 skilled in the art without departing from the scope of the present
15 invention which is only limited by the appended claims. Therefore, the
16 embodiment shown and described is only illustrative, not restrictive.

What is claimed is:

1 1. A method for transmitting HDLC (high level data link control)
2 variable-length packets and non-HDLC fixed-length packets over a
3 common transmission medium, comprising:
4 a) decomposing each of said HDLC variable-length packets and
5 each of said non-HDLC fixed-length packets into one or more cells;
6 b) generating a cell identifier for each of said cells, said cell
7 identifier identifying type of the packet from which said cell is
8 decomposed;
9 c) transmitting a frame sync code from one end of said
10 transmission medium;
11 d) assembling said cell identifier and each of said cells into a field
12 and assembling a plurality of said fields into a frame, and transmitting
13 the frame through said transmission medium;
14 e) detecting said frame sync code at the other end of said
15 transmission medium as a timing reference and deassembling said
16 frame into the fields in response to said timing reference;
17 f) deassembling each of the fields into a cell identifier and a cell;
18 and
19 g) composing the deassembled cells into the original HDLC
20 variable-length packet or non-HDLC fixed-length packet according to
21 the deassembled cell identifier.

1 2. A method as claimed in claim 1, wherein said cell identifier is a
2 block code comprising cell identification bits identifying said type and
3 error correcting bits, wherein the step (f) comprises correcting error
4 contained in said cell identification bits of each cell identifier using the

5 error correcting bits of the cell identifier.

1 3. An integrated communications system comprising:
2 an HDLC (high level data link control) variable-length packet
3 transmitter;
4 a non-HDLC fixed-length packet transmitter;
5 a transmit shift register having an input terminal connected to said
6 packet transmitters and an output terminal connected to one end of a
7 transmission medium;
8 a sync generator for supplying a sync code to said transmit shift
9 register at periodic intervals;
10 a header generator;
11 cell formatting means for activating for a predetermined period one
12 of said packet transmitters having a packet to transmit so that a portion
13 of said packet is supplied to said shift register as a cell, causing said
14 header generator to supply a cell identifier identifying type of the packet
15 from which said cell is decomposed to said transmit shift register to form
16 a field with said cell, and causing said transmit shift register to assemble
17 said sync code and a plurality of said fields into a frame for transmission
18 through said transmission medium;
19 a receive shift register having an input terminal connected to the
20 other end of said transmission medium, said receive shift register being
21 supplied with said transmitted frame;
22 a sync detector for detecting the sync code contained in the frame
23 supplied to said receive shift register;
24 a header detector responsive to the detection of a sync code by
25 said sync detector for detecting the cell identifier of each field of the
26 frame in said receive shift register;

27 an HDLC variable-length packet receiver;
28 a non-HDLC fixed-length packet receiver; and
29 cell deformatting means responsive to the cell identifier detected by
30 said header detector for activating for said predetermined period one of
31 said packet receivers identified by said detected cell identifier so that
32 said portion of said packet is supplied from said receive shift register to
33 said one of the packet receivers.

1 4. An integrated communications system as claimed in claim 3,
2 wherein said cell formatting means assembles cells from said HDLC
3 variable-length packet transmitter with cells from said non-HDLC fixed-
4 length packet transmitter in a common frame.

1 5. An integrated communications system as claimed in claim 3,
2 wherein said cell identifier is encoded with error correcting bits, wherein
3 said header detector corrects an error contained in said cell identifier
4 using said error correcting bits.

1 6. An integrated communications system as claimed in claim 3,
2 wherein said header detector comprises a memory for storing 2^n bits,
3 where n indicates a total number of bits contained in said cell identifier
4 and reading one of said stored 2^n bits in response to said cell identifier.

1 7. An integrated communications system as claimed in claim 3,
2 further comprising a flag generator for generating a predetermined bit
3 pattern, wherein said cell formatting means causes said flag generator to
4 supply said bit pattern to said shift register as a cell in the absence of a
5 packet to transmit in any of said packet transmitters.

1 8. An integrated communications system as claimed in claim 3,
2 wherein said non-HDLC fixed-length packet transmitter comprises:
3 a short-length packet transmitter for transmitting a short packet
4 having a length equal to the length of said cell; and
5 a long-length packet transmitter for transmitting a long packet
6 having a length equal to an integral multiple of the length of said cell,
7 wherein said cell identifier identifies different cells of said long packet
8 with respective cell identifiers, wherein said fixed-length packet receiver
9 comprises:
10 a short-length packet receiver for assembling the cells identified by
11 said cell identifier into said short packet; and
12 a long-length packet receiver for assembling the cells identified by
13 said respective cell identifiers into said long packet.

1 9. An integrated communications system as claimed in claim 8,
2 wherein said long packet comprises an integral multiple of the number
3 of bits contained in said short packet.

1 10. An integrated communications system as claimed in claim 3,
2 further comprising means for selecting one of said packet transmitters
3 according to a predetermined priority algorithm and causing said cell
4 formatting means to activate said selected one of said packet
5 transmitters for said predetermined duration.

1 11. An integrated communications system as claimed in claim 3,
2 wherein said cell formatting means continuously drives said shift
3 registers with clock pulses and drives said one of said packet transmitters

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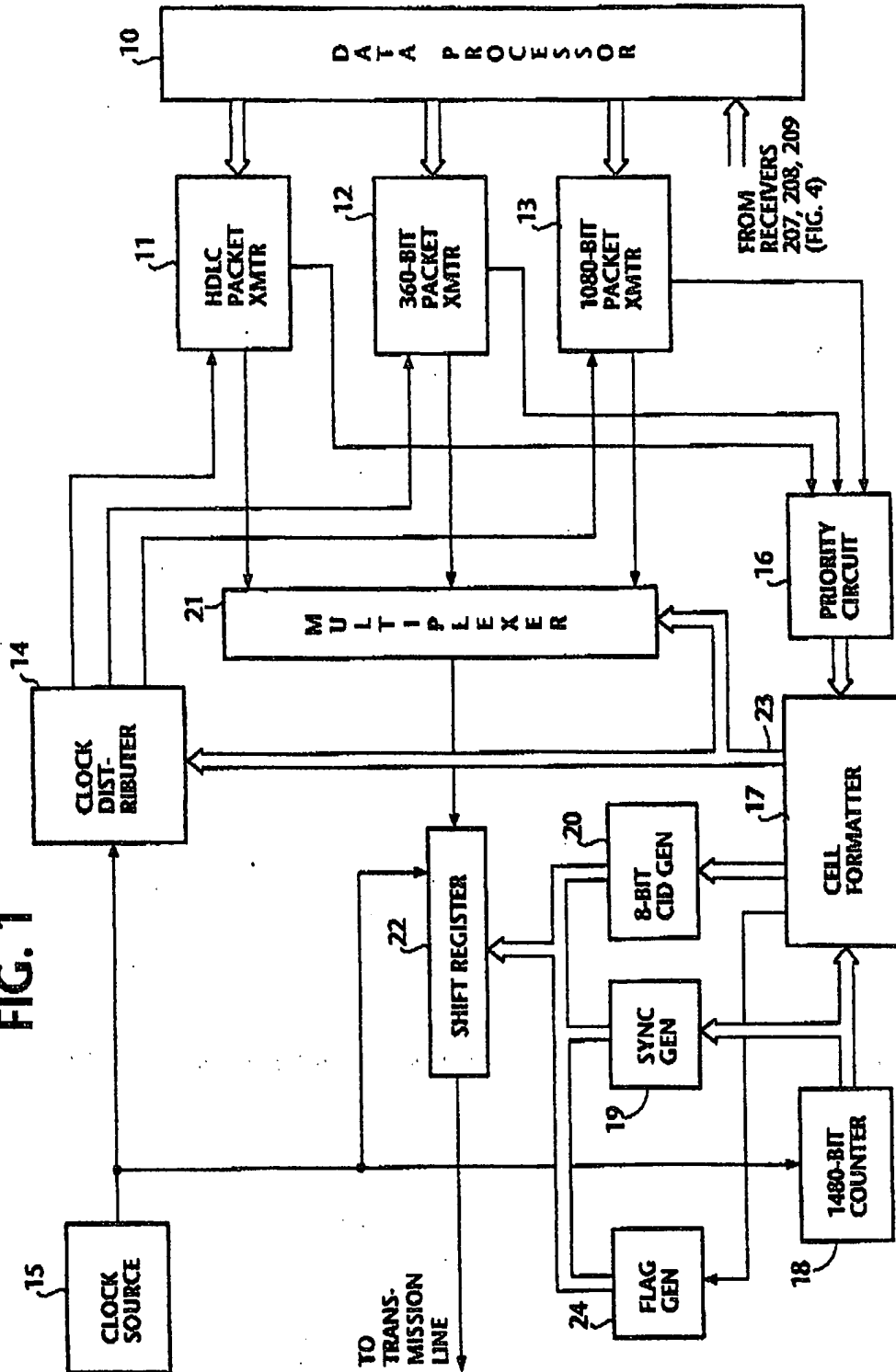
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- 4 with said clock pulses for said predetermined duration to transfer bits
- 5 from the driven packet transmitter to said shift register.

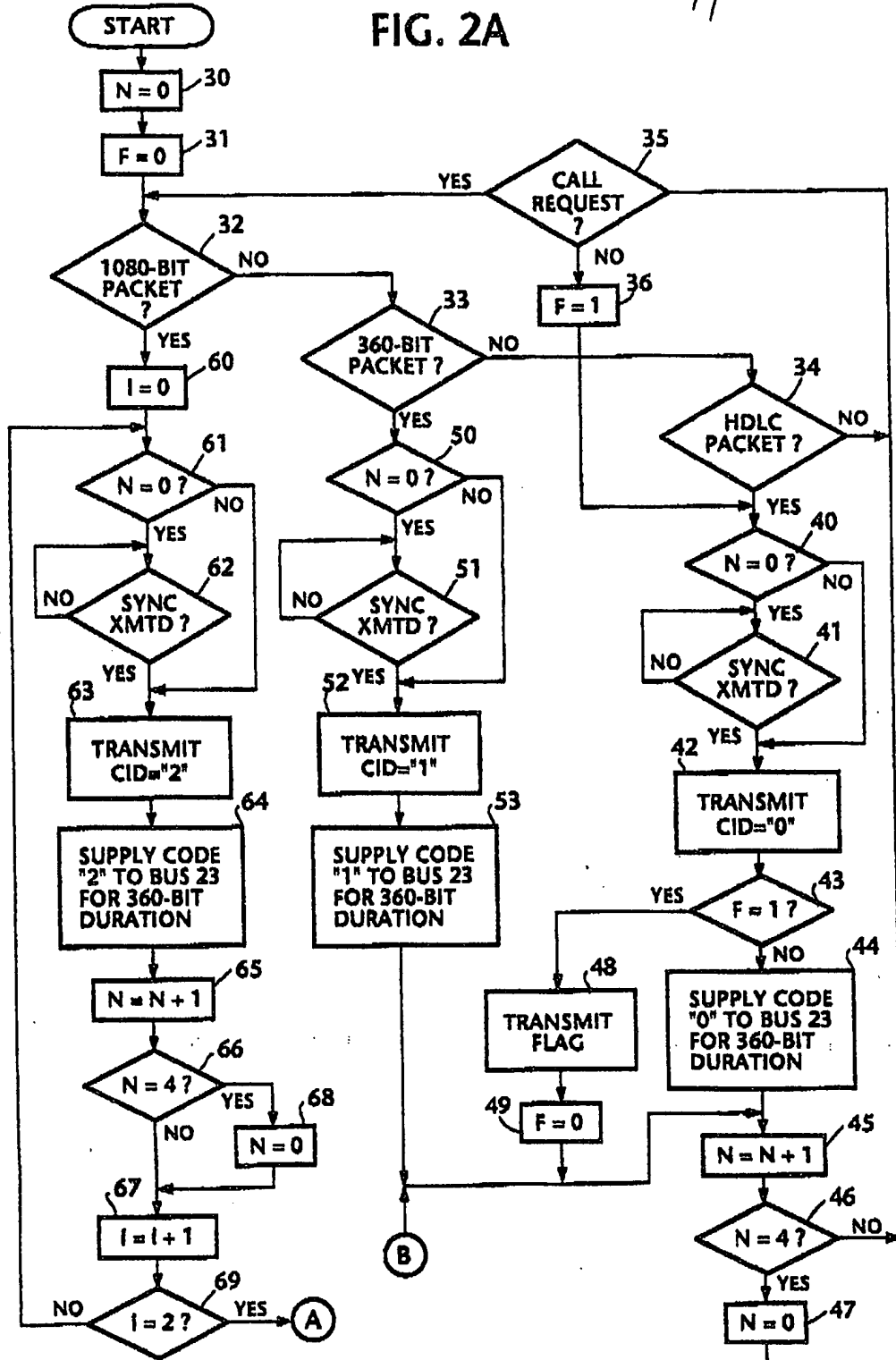


FIG. 1



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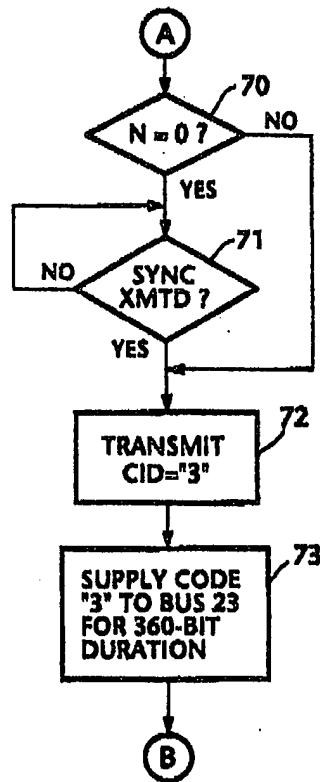
FIG. 2A



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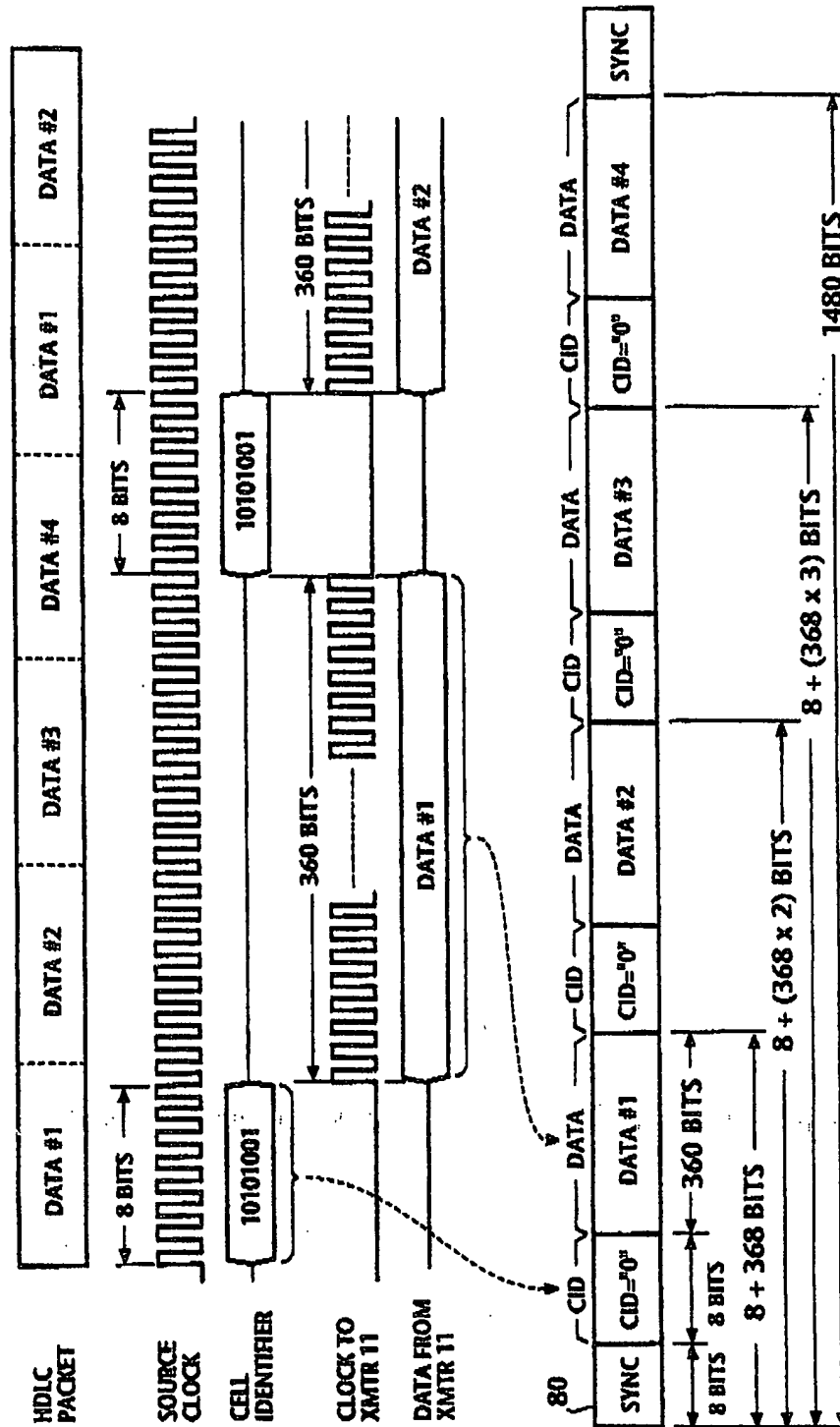
FIG. 2B



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FIG. 3A



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FIG. 3B

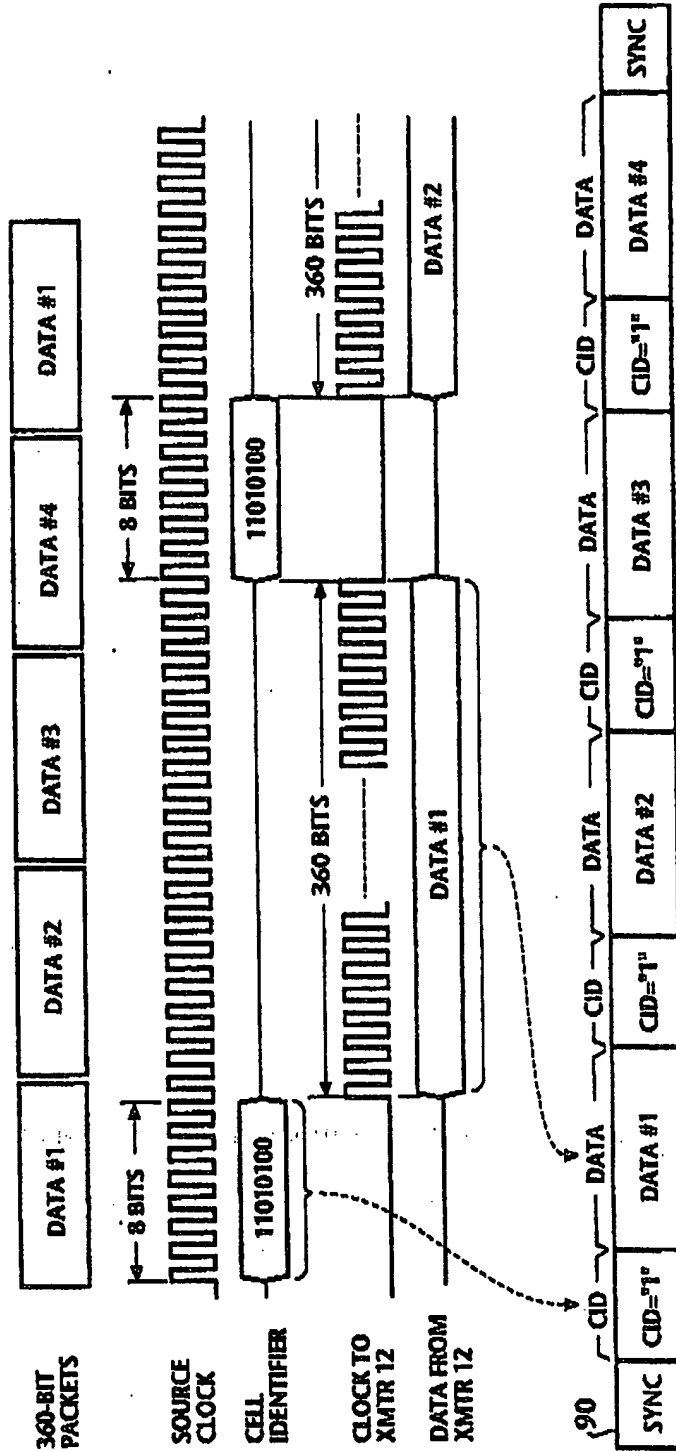


FIG. 3C

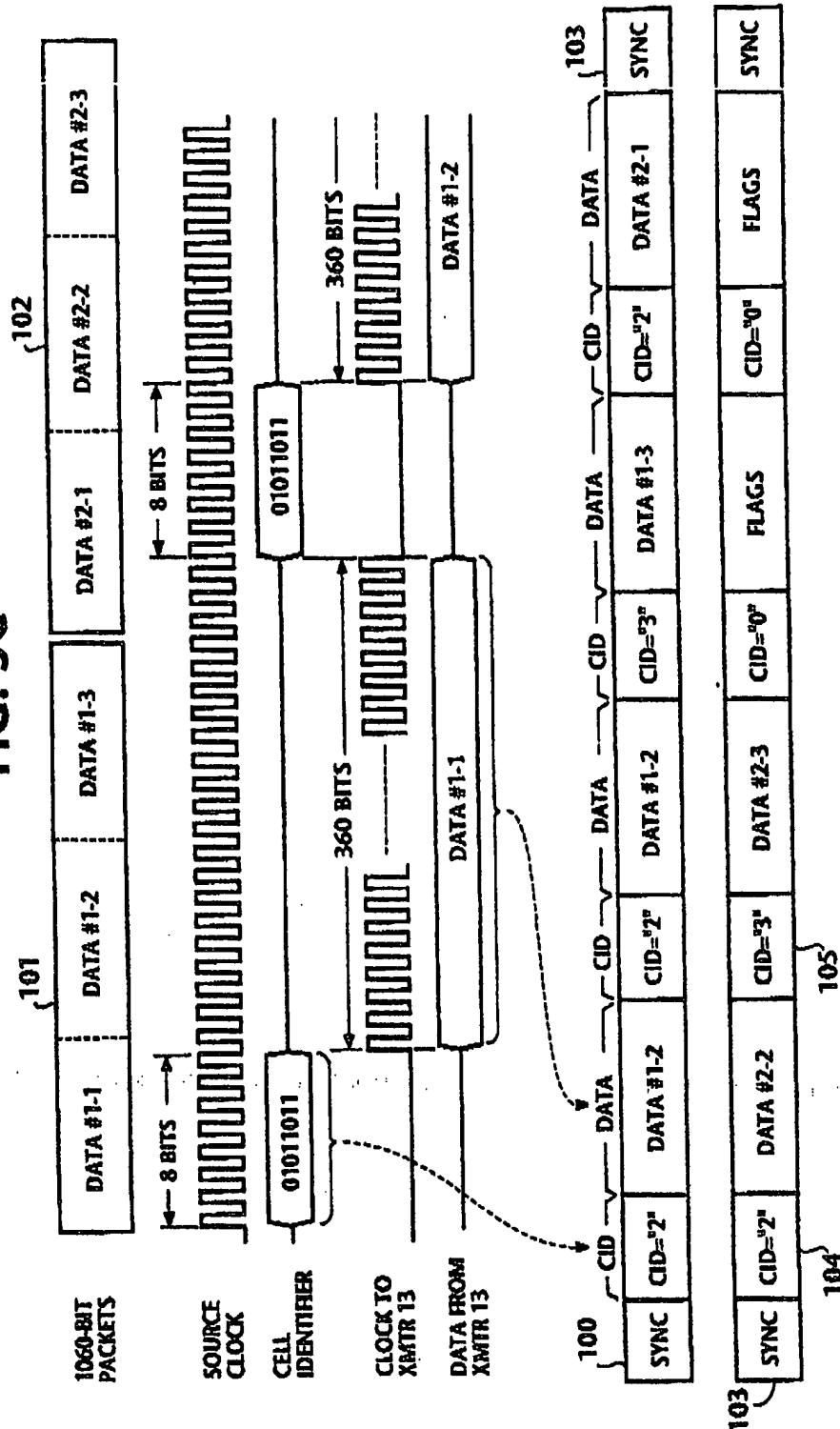
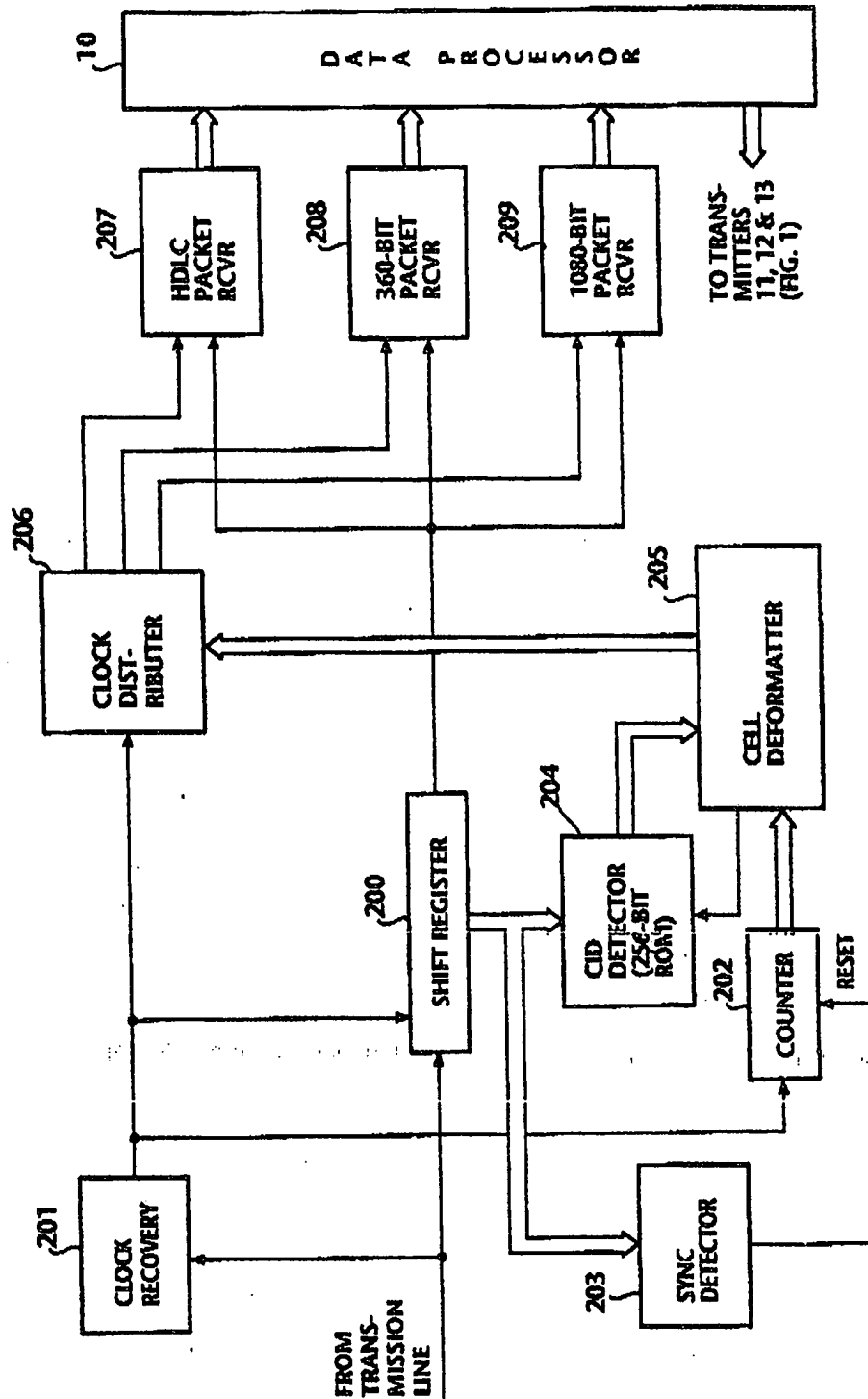


FIG. 4



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